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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,275	09/19/2003	CHI-HSING HSU	11241-US-PA	2274

31561 7590 06/30/2004

JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
ROOSEVELT ROAD, SECTION 2
TAIPEI, 100
TAIWAN

EXAMINER
PAREKH, NITIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 06/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,275	HSU, CHI-HSING	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

2. Claims 1, 3, 5-7 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US Pat. Application Publication 2003/0151139) in view of admitted prior art (APA).

Regarding claims 1, 3, 5 and 9, Kimura discloses a resin sealed leadless flat package/no-lead chip carrier (see Fig. 1 and 7) comprising:

- a metal substrate (MS)/conductive plate (CP 109 in Fig. 1 and 7) having a first/top surface and a second/bottom surface
- the first/top surface has a chip-bonding region (see area under 101 in Fig. 1 and 7), the first/top surface and the second/bottom surface having an oxide layer thereon (see 108 in Fig. 1 and 7; section 0028) and

- the MS/CP has a plurality of columnar through holes having column/funnel shape (see 112/113, 211/311 and 212/312 in Fig. 1-7), the through holes being located on the periphery of the chip-bonding region such that the through holes pass through the MS/CP to link up the first/top and the second/bottom surfaces
- a plurality of conductive columns (see 110/111 in Fig. 1 and 7; section 0031 and 0033) set up within the respective columnar through holes
- a plurality of insulating/dielectric walls (see 108 and 608 in Fig. 1-7) set up between the sidewall of the conductive columns and the inner surface of corresponding columnar through holes
- a chip attached (101 in Fig. 1 and 7) to the chip-bonding region on the first/top surface of the MS/CP
- a plurality of first conductive wires (102 in Fig. 1 and 7) electrically connecting the chip and the conductive columns, and
- an insulating resin material (103 in Fig. 1 and 7) enclosing the chip and the first wires

(Fig. 1 and 7; Fig. 1-7; sections 0026-0040).

Kimura fails to teach the chip carrier being in a quad flat chip carrier (QFCC) configuration.

Admitted Prior Art (APA) teaches a chip carrier in a conventional non-leaded QFCC configuration (see Fig. 1A/1B; sections 0006-0008).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the chip carrier being in the quad flat chip carrier configuration as taught by the APA so that wiring density can be increased in Kimura's chip carrier.

Regarding claim 6, Kimura and APA teach the entire claimed structure as applied to claim 5 above, except the package further comprising at least a second conductive wire electrically connecting the chip to the conductive plate.

The APA teaches using a second conductive wire electrically connecting the chip to the conductive plate (see 132 in Fig. 1A; section 0006).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate at least a second conductive wire electrically connecting the chip to the conductive plate as taught by the APA so that a grounding can be provided in APA and Kimura's chip carrier.

Regarding claim 7, Kimura and APA teaches the entire claimed structure as applied to claim 5 above, except the package further comprising a conductive paste layer sandwiched between the chip and the conductive plate.

The APA teaches using a conductive paste/silver epoxy being sandwiched between the chip and the conductive plate (see 118 in Fig. 1A; section 0006).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the conductive paste layer sandwiched between the chip and the conductive plate as taught by the APA so that the chip adhesion can be improved in APA and Kimura's chip carrier.

3. Claims 2 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US Pat. Application Publication 2003/0151139) and APA as applied to claims 1 and 5 above, and further in view of Kikuchi et al. (US Pat. 5122860).

Regarding claims 2 and 8, Kimura and APA teach the entire claimed structure as applied to claims 1 and 5 above, except the first surface of the conductive plate being a rough surface.

Kikuchi et al. teach a flat package having a CP/MS (see 11 in Fig. 6 and 7 where a top surface of the CP has a rough surface (see 11b in Fig. 6 and 7) to provide an improved resin adhesion (Col. 6, lines 50-60).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first surface of the conductive plate being rough as taught by Kikuchi et al. so that the resin adhesion can be improved in the APA and Kimura's chip carrier.

4. Claims 4 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kimura (US Pat. Application Publication 2003/0151139) and APA as applied to claims 1 and 5 above, and further in view of Murata (US Pat. 6400010).

Regarding claims 4 and 10, Kimura and APA teach the entire claimed structure as applied to claims 1 and 5 above, wherein Kimura teaches another embodiment where the second surface of the CP comprises an insulating layer (see 923 in Fig. 9; sec. 0038-0040) near an exposed conductive portion on the second/bottom surface to provide the desired surface protection, but fail to teach using a solder mask layer.

Murata teaches using a conventional solder mask as an insulating layer on top and bottom surfaces of a substrate (see 24 in Fig. 2B; Col. 8, line 54).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the solder mask layer near the exposed conductive portion as taught by Murata so that the desired degree of surface protection can be achieved in the APA and Kimura's chip carrier.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Nitin Parekh

Nitin Parekh

PATENT EAMINER

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NP

06-22-04